

## **REMARKS**

This responds to the Office Action mailed on February 3, 2006. Claim 4 is amended and claim 3 is canceled by way of this Amendment.

### **Claim Objections**

Claim 3 is objected to because “substantially simultaneously” renders the claim confusing. Claim 4 is objected to because of its dependency from claim 3. Claim 3 is canceled and claim 4 is amended to depend from claim 1. The objections are believed to be overcome. Withdrawal of the objections is respectfully requested.

### **§103 Rejection of the Claims**

Claims 1-5, 20-21 stand rejected under 35 USC § 103(a) as being unpatentable over Beat (US Pat. No. 6,912,173) and Brown (US Pat. No. 6,434,657).

Independent claim 1 recites a method that includes writing a first and a second portions of a first block of the data to a first and second memory banks of the memory unit, depending on whether the data is aligned or not aligned, respectively.

In contrast, Beat discloses a system that provides two separate physical memories each being 64-bits wide (col. 2, lines 47-48). Beat notes that “a particular microcomputer may have a sixty-four bit wide memory, but may be required to access and manipulate eight-bit, sixteen-bit, thirty-two bit and sixty-four bit data.” (Col. 2, lines 31-34). Thus Beat’s 64-bits wide memory allows for data that is aligned to be written into a single memory location in only one of the separate physical memories.

The Examiner notes that the motivation to combine Beat and Brown is to “eliminate holes in the address space arising from writing word widths that are not a power of 2 times the read word width” (citing Brown, col. 1, lines 22-37). However, to modify the system in Beat “to write the 1<sup>st</sup> data portion into the even memory section and the 2<sup>nd</sup> data portion into the odd memory section in Beat as taught in Brown” would result in the exact problem that Brown sought to address. That is, holes in the address space when the data (eight-, sixteen-, thirty-two and sixty-four bit data as specified by Beat) is aligned because each of Beat’s two memories is 64-bits wide. In other words, if 8/16/32/64-bit data is aligned, then the data would fit in a

location within one of the physical memories and to force the aligned data to span two locations in the two physical memories would create holes in the address space.

Independent claim 5 recites a system including logic that selects a first (or second) portion of a first block of data to be written to the first memory bank if the first block of data is aligned (or not aligned) and logic that selects the first (or second) portion of the first block of data to be written to the second memory bank if the first block of data is not aligned (or aligned). As such, the discussion regarding claim 1 above similarly applies to independent claim 5.

Independent claim 20 recites a method that, if the starting memory address is even (or odd), writes a first and second portion of a first data block in the sequence to a first (or second) and second (or first) memory bank at a location identified by a first address. As such, the discussion regarding claim 1 above similarly applies to independent claim 20.

Withdrawal of the rejection of independent claims 1, 5, and 20 as well as claims 2-4 and 21 dependent variously therefrom is respectfully requested.

Dependent claims 6-8 and 22-24 stand rejected under 35 USC § 103(a) as being unpatentable over Beat and Brown, and further in view of Melaragni, Wolrich, Wertheizer, Tomita, Cho, or Burroughs. However, because independent claims 5 and 20 from which these claims various depend are believed to be allowable new and non-obvious over Beat and Brown, dependent claims 6-8 and 22-24 are also believed to be allowable at least for the same or similar reasons as discussed above. Withdrawal of the rejection of claims 6-8 and 22-24 is respectfully requested.

Claims 9, 10, and 13 stand rejected under 35 USC § 103(a) as being unpatentable over Wertheizer and Brown 2.

Independent claim 9 recites a system having first and second multiplexors whose outputs are communicatively connected to the first and second memory banks and operable to select between first and second portions of a first data block based on whether the first data block is aligned, and to pass the selected portion to the first and second memory banks, respectively. The system also includes a third multiplexor whose output is communicatively coupled to an address input of the first memory bank, and operable to select between a first and second address based

on whether the first data block is aligned, and to pass the selected address to the address input of the first memory bank.

In contrast, neither Wertheizer nor Brown 2, either alone or in combination discloses or suggests having two multiplexors (first and second multiplexors) that select between first and second portions of a first data block based on whether the first data block is aligned, and to pass the selected portion to the first and second memory banks, respectively. Accordingly, withdrawal of the rejection of independent claim 9 and claims 10 and 13 (dependent from claim 9) is respectfully requested.

Dependent claims 11, 12, and 14-19 stand rejected under 35 USC § 103(a) as being unpatentable over Wertheizer and Brown 2, and further in view of Norman, Roth, applicant's admitted prior art, Sugita, Melaragni, and/or Wolrich. However, because independent claim 9 from which these claims depend is believed to be allowable new and non-obvious over Wertheizer and Brown, dependent claims 11, 12, and 14-19 are also believed to be allowable at least for the same or similar reasons as discussed above. Withdrawal of the rejection of claims 11, 12, and 14-19 is respectfully requested.

Claims 25 and 27 stand rejected under 35 USC § 103(a) as being unpatentable over Beat, Brown, and Wybenga.

Independent claim 25 recites a system having logic for selecting data to be written to the first and second memory bank and operable to select a first portion of a first block of data if the first block of data is aligned (or not aligned), and to select a second portion of the first block of data if the first block of data is not aligned (or aligned), respectively. As such, the discussion regarding claim 1 above similarly applies to independent claim 25.

However, the addition of the Wybenga reference does not overcome the deficiencies of the combination of Beat in view of Brown as discussed above with reference to independent claim 1. Thus, withdrawal of the rejection of claims 25 and 27 (dependent from independent claim 25) is respectfully requested.

Dependent claim 26 stands rejected under 35 USC § 103(a) as being unpatentable over Beat, Brown, Wybenga and further in view of Wertheizer. However, because independent claim 25 from which claim 26 depends is believed to be allowable new and non-obvious over Beat, Brown and Wybenga, dependent claim 26 is believed to be allowable at least for the same or similar reasons as discussed above. Withdrawal of the rejection of claim 26 is respectfully requested.

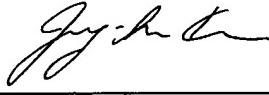
**Conclusion**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (650-988-8070) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-1217.

Respectfully submitted,  
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By: 

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